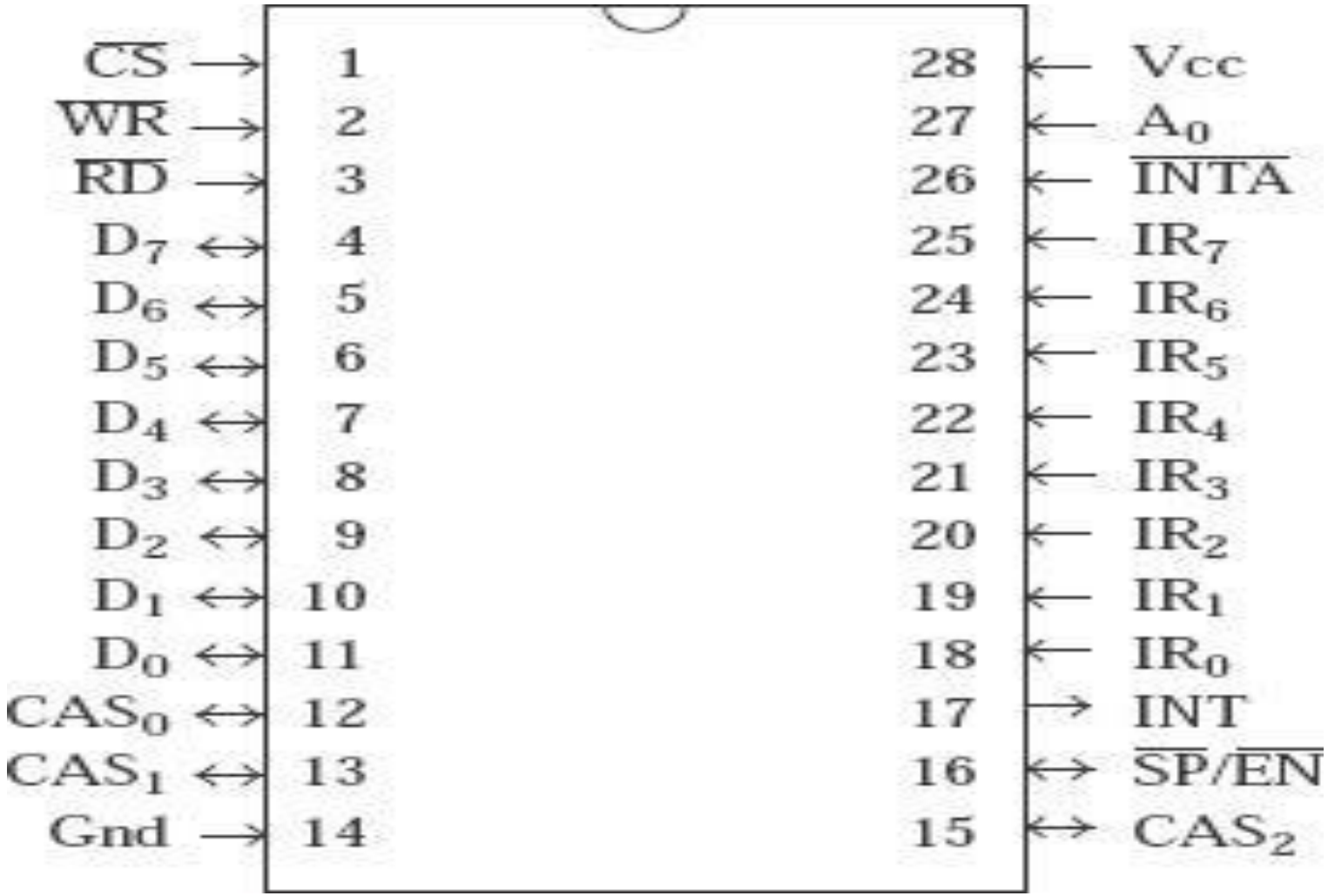
8259A

PROGRAMMABLE INTERRUPT CONTROLLER

Characteristics of 8259A:

- 8259A is known as PIC
- N-MOS technology is used in the device
- Contains 28 pins
- Implement the interrupt interface in a microprocessor
- It is treated as peripheral device
- Compatible with 8-bit and 16-bit microprocessor
- It can be programmed either in edge triggered, or in level triggered mode
- Clock cycle is not needed
- It adds eight vectored priority encoded interrupt to the microprocessor
- The controller can be expanded to 64 bit interrupt request input. This expansion requires a master 8259 and eight 8259 slaves

PIN CONFIGURATION


$\overline{CS}$ → 1
$\overline{WR}$ → 2
$\overline{RD}$ → 3
D_7 ↔ 4
D_6 ↔ 5
D_5 ↔ 6
D_4 ↔ 7
D_3 ↔ 8
D_2 ↔ 9
D_1 ↔ 10
D_0 ↔ 11
CAS_0 ↔ 12
CAS_1 ↔ 13
Gnd → 14
28 ← Vcc
27 ← A_0
26 ← $\overline{INTA}$
25 ← IR_7
24 ← IR_6
23 ← IR_5
22 ← IR_4
21 ← IR_3
20 ← IR_2
19 ← IR_1
18 ← IR_0
17 → INT
16 ↔ $\overline{SP}/\overline{EN}$
15 ↔ CAS_2

VCC:
*5-V supply

GND:
*Ground pin

CS(Chip Select):
*A active low pin
*this pin enables RD and WR operation between CPU and 8259

WR(Write):
*A active low pin
*When CS is low , enables 8259 for write operation
*Also enables to accept command words from the CPU

RD(Read):
*A active low pin
* Enables 8259 to release status onto the data bus for the CPU

D7-D0(I/O Bi-directional Data Bus) :
*Used as bi-directional data bus
*Transfer the control , status and interrupt-vector information through this bus

CAS0-CAS2 (I/O Cascade Lines):
*It is used to control a multiple 8259A structure
*These pins are outputs for a master 8259A and inputs for a slave 8259A

SP/EN(I/O Slave Program/Enable Buffer):
*A dual function pin
*A active low pin
*When it is used in buffer mood , it can be used as an output to control buffer transceivers(EN)
*If it is not in buffer mood , it is used as an input to designate a master (SP=1) or slave (SP=0)

INT(Interrupt):
*A active high pin
*Used to interrupt the CPU

IR0-IR7(Interrupt Request):

*There are Eight asynchronous interrupt request inputs
*These interrupt requests can be programmed for level-trigger or edge-triggered mode.

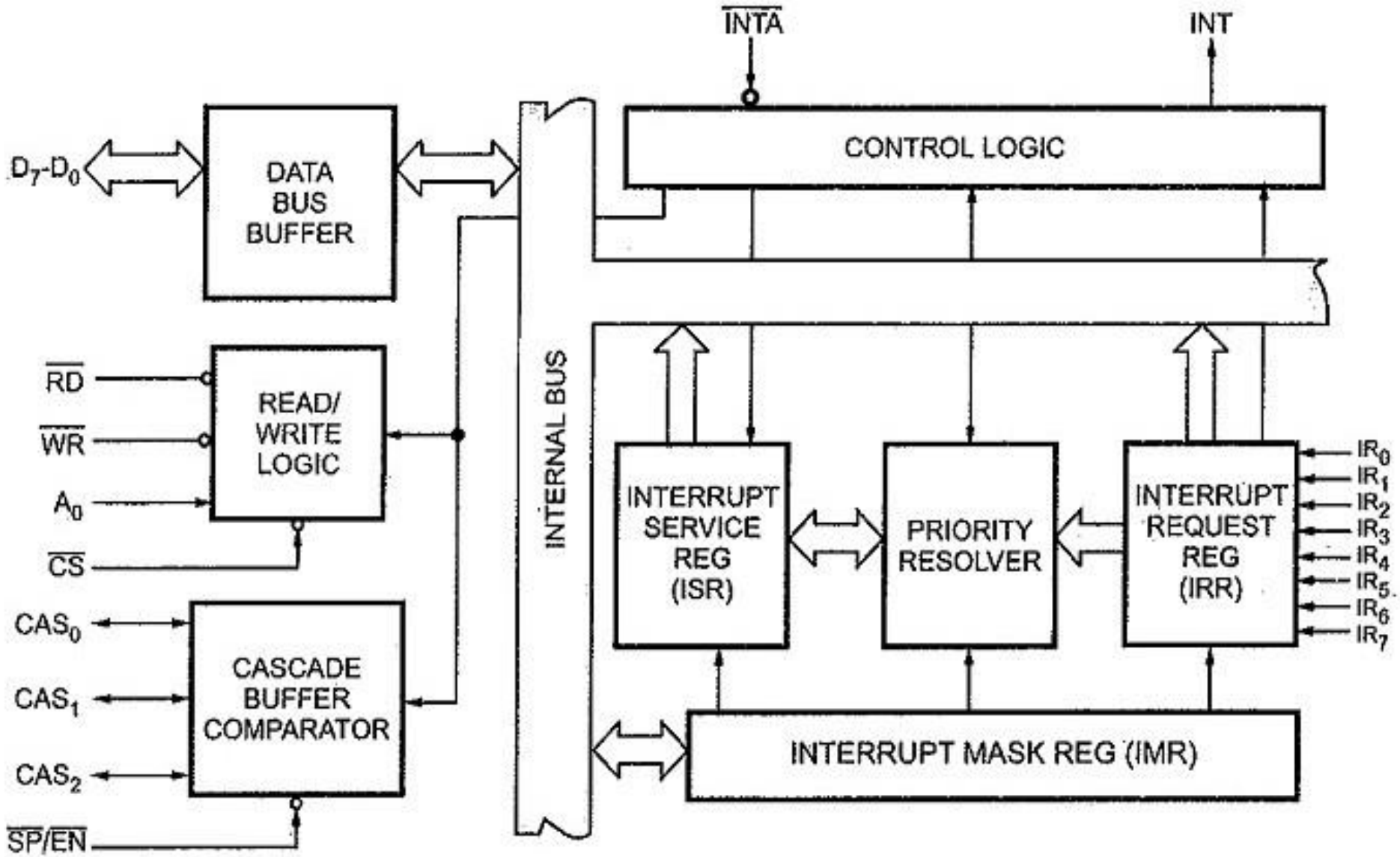
INTA(Interrupt Acknowledge):

*This pin is active high when a valid interrupt request is asserted
*use to enable 8259A interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulse issued by the CPU

A0(Address Line):

*Works in the conjunction with the CS , WR and RD pins
*Used to read various commands words the CPU writes and the status the CPU wishes to read by 8259A
*Connected to the CPU A0 address line

BLOCK DIAGRAM


INTA
INT
CONTROL LOGIC
D_7-D_0
DATA BUS BUFFER
INTERNAL BUS
RD
WR
A_0
CS
READ/ WRITE LOGIC
INTERRUPT SERVICE REG (ISR)
PRIORITY RESOLVER
INTERRUPT REQUEST REG (IRR)
IR_0
IR_1
IR_2
IR_3
IR_4
IR_5
IR_6
IR_7
CAS_0
CAS_1
CAS_2
CASCADE BUFFER COMPARATOR
SP/EN
INTERRUPT MASK REG (IMR)

Data bus buffer:

By acting as a buffer ,this Block is used as a mediator between 8259 and 8086.The data bus buffer consists of 8 bits represented as D0-D7 in the block diagram. Thus, shows that a maximum of 8 bits data can be transferred at a time.

Read/Write logic :

This block works only when the value of pin CS is low. This block is responsible for the flow of data depending upon the inputs of RD and WR. RD and WR pins are used for read and write operations. And A0 is only selection line.

Control logic:

It is the centre of the microprocessor and controls the functioning of every block. It has pin INTR which is connected with 8086 for taking interrupt request and pin INT for giving the output.

Cascade buffer:

To increase the Interrupt handling capability, we can further cascade more number of pins by using cascade buffer. So, during increment of interrupt capability, CSA lines are used to control multiple interrupt structure.

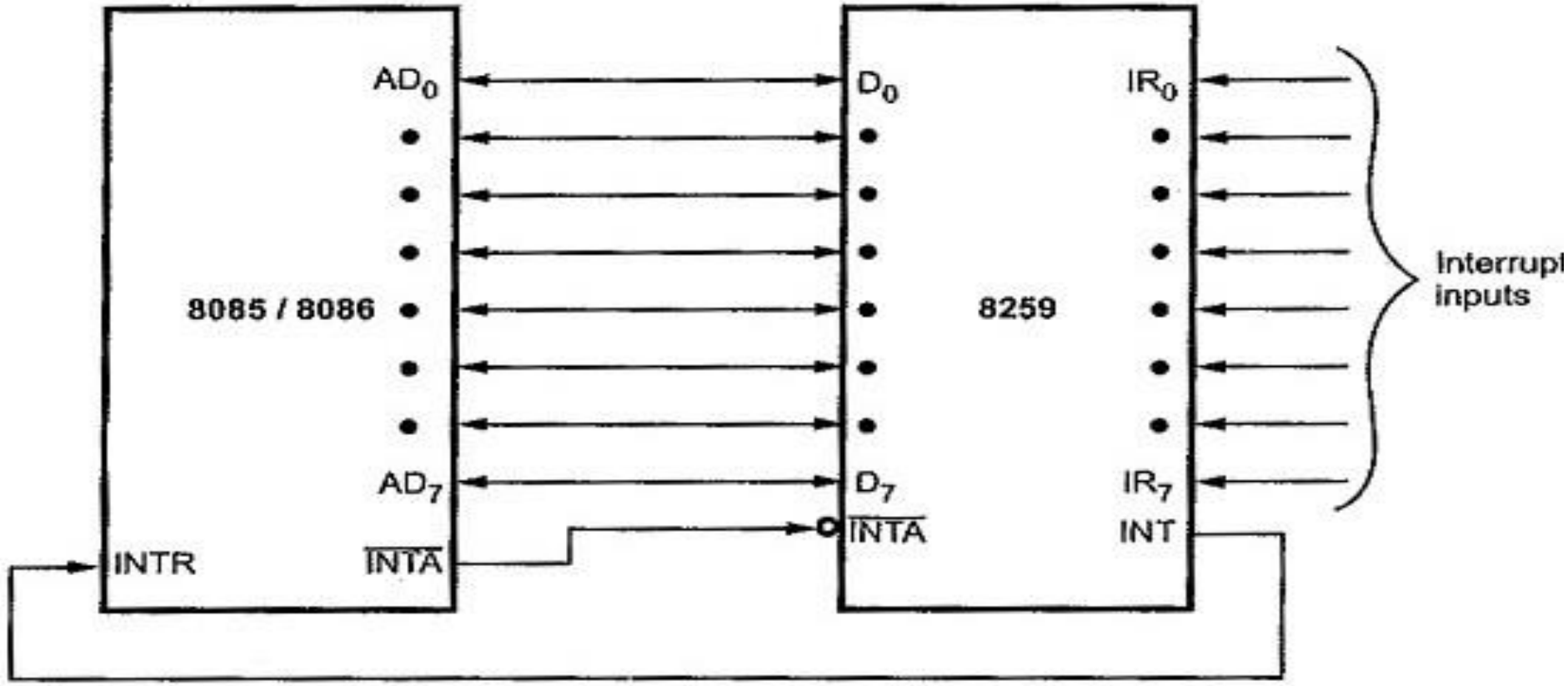
Interrupt request register (IRR):
It stores all the interrupt level which are requesting for Interrupt services.

Interrupt service register (ISR):
It stores the interrupt level which are currently being executed.

Interrupt mask register (IMR):
It stores the interrupt level which have to be masked by storing the masking bits of the interrupt level.

Priority resolver:
It examines all the three registers (IRR,ISR,IMR) and set the priority of interrupts and according to the priority of the interrupts, interrupt with highest priority is set in ISR register.

8259A interfacing with 8086



*The data lines of an 8259 are connected to the lower half of the system data bus; because the 8086 expects to receive interrupt types on these lower eight data lines

*The interrupt request signal INT from the 8259 is connected to the INTR input of the 8086

*INTA from the 8086 is connected to INTA on the 8259A.

USE OF 8259A:

* Interrupts can be a powerful mechanism for servicing data acquisition and control operations. With interrupts, the processor can respond quickly and efficiently to data acquisition hardware.
* Simply transferring acquired data, interrupts can be used to synchronize different events, or process data as it is acquired.
* The PC design uses the Intel 8259A programmable interrupt controller to provide several prioritized interrupts for the I/O bus.